

# Cache & Virtual Memory Simulator

Web-app simulator for educational purposes

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### Cache Simulation

**Setup**

Explanation  
The CPU then proceeds to read the required byte at address 0x8.

Hit: 5, Miss: 3

Address Sequence: 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9

Tag	Block	Content
00	00	@0x0 @0x1 @0x2 @0x3
00	01	@0x4 @0x5 @0x6 @0x7
00	10	@0x8 @0x9 @0xa @0xb
Empty	11	

Block	Content
0	@0x0 @0x1 @0x2 @0x3
1	@0x4 @0x5 @0x6 @0x7
2	@0x8 @0x9 @0xa @0xb
3	@0xc @0xd @0xe @0xf
4	@0x10 @0x11 @0x12 @0x13
5	@0x14 @0x15 @0x16 @0x17
6	@0x18 @0x19 @0x1a @0x1b
7	@0x1c @0x1d @0x1e @0x1f
8	@0x20 @0x21 @0x22 @0x23
9	@0x24 @0x25 @0x26 @0x27
10	@0x28 @0x29 @0x2a @0x2b
11	@0x2c @0x2d @0x2e @0x2f
12	@0x30 @0x31 @0x32 @0x33
13	@0x34 @0x35 @0x36 @0x37
14	@0x38 @0x39 @0x3a @0x3b
15	@0x3c @0x3d @0x3e @0x3f

Current Address: 0x20

Main Memory Address: 0x40

0xc

Next explanation

Prev explanation

Next Address

Prev Address

Restart

### Virtual Memory Simulation

**Setup**

Explanation  
Since there was a TLB miss, the page table is looked up. The page table entry at row 0 has a valid bit of 0, hence there is a page fault. This means that the data being accessed is not in the Physical Memory and must be brought in from the Storage Memory.

Address Sequence: 0x0, 0x20, 0x40, 0x60, 0xc

Virtual Page Number	Physical Frame Number
2	0
3	1
-	-
-	-

Index	Frame Number	Valid Bit
0	0	0
1	1	0
2	0	1
3	1	1

Hit: 0, Miss: 5

Frame	P2W0	P2W1	P2W2	P2W3	P2W4	P2W5	P2W6	P2W7
Frame 0	P2W8	P2W9	P2W10	P2W11	P2W12	P2W13	P2W14	P2W15
	P2W16	P2W17	P2W18	P2W19	P2W20	P2W21	P2W22	P2W23
	P2W24	P2W25	P2W26	P2W27	P2W28	P2W29	P2W30	P2W31
	P3W0	P3W1	P3W2	P3W3	P3W4	P3W5	P3W6	P3W7
Frame 1	P3W8	P3W9	P3W10	P3W11	P3W12	P3W13	P3W14	P3W15
	P3W16	P3W17	P3W18	P3W19	P3W20	P3W21	P3W22	P3W23
	P3W24	P3W25	P3W26	P3W27	P3W28	P3W29	P3W30	P3W31

## Project Objectives:

Web app to simulate cache and virtual memory management operation and performance analysis. The application features simulation of Direct-Mapped, Set Associative and Fully Associative Mapping Scheme for Cache. Address sequence can be entered manually or via a script file. Memory structures are fully configurable. Cache Memory Performance Analysis can also be simulated over a large real workload dataset to be compared amongst different configurations.

## Additional Features:

- Single stepping (forward and backward) feature
- Virtual Memory Demand Paging and TLB integration
- In-step text-based commentary

## Analysis page

