NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

School of Computer Science and Engineering
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Automatic Generation of Approximate Arithmetic Circuits for Error-Tolerant Computing

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Introduction

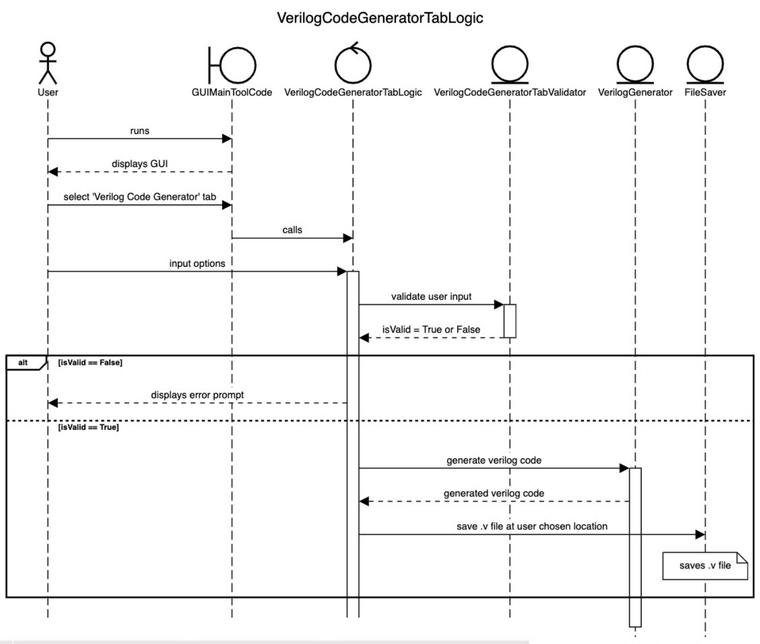
In recent years, the amount of data produced daily has been increasing. Because of that there is now a need for techniques to speed up the processing of data while warranting that the accuracy of result is within acceptable bounds of application domain. To put it another way, to decrease the time taken for computation while ensuring that loss in accuracy is kept to minimal. Especially so in image processing domain.

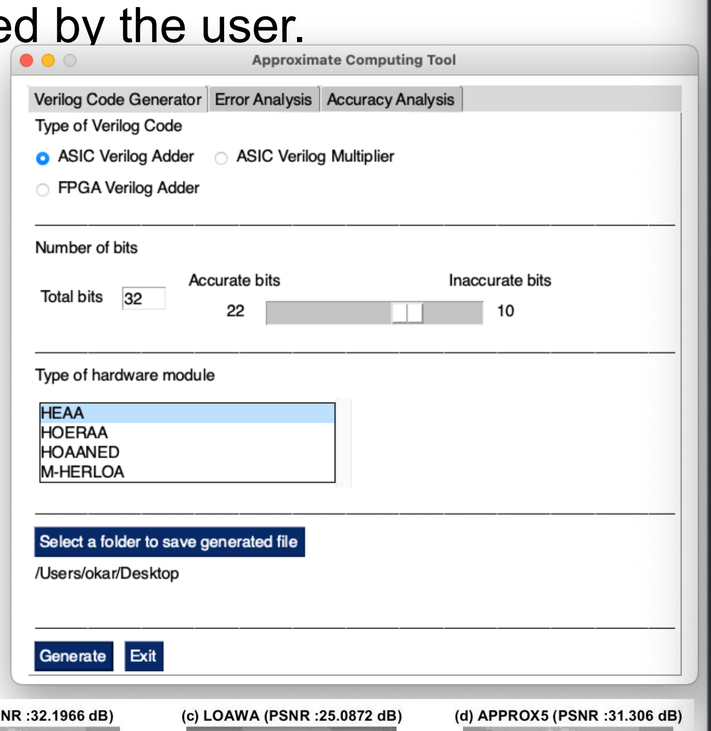
Objective

To develop a user-friendly Graphical User Interface (GUI) tool which uses input provided by the user to generate Verilog codes of different approximate arithmetic circuits architectures, compute error-analysis and accuracy-analysis of those architectures.

Tool Overview

1. **Verilog Code Generator** : Generate and save Verilog hardware description language file for chosen approximate arithmetic architecture (.v file).
2. **Error Analysis** : Compute mean square error (MAE) and root mean square error (RMSE) using 1,000,000 random inputs to chosen approximate arithmetic architecture.
3. **Accuracy Analysis**: Compute percentage of accuracy of an approximate arithmetic architecture using two values provided by the user.





Approximate Adder	Error Metrics	
	Average Error (AE)	Root Mean Square Error (RMSE)
LOA	0.136	256.097
LOAWA	–255.580	361.592
APPROX5	0.706	295.680
HEAA	–127.722	180.842
OLOCA	63.917	276.672
HOERAA	–32.106	165.320
HOAANED	0.002	165.210